Design and Characterization of Integrated Passive Elements on High Ohmic Silicon

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***Abstract* —This work presents ultra low-loss co-planar waveguides and Marchand type baluns implemented in an optimized high ohmic silicon substrate technology for RF/ microwave applications. The CPW configured baluns operate from 15 to 25GHz with a minimum insertion loss of 0.8 dB at center frequency.**

I. INTRODUCTION

With the recent speed improvements of the active silicon devices (f_T & f_{Max} > 200GHz [1]), the integration of high performance passives at mm-wave frequencies has become very important for the enabling high-volume, low-cost monolithic RF/microwave circuit solutions. However, the low-resistivity silicon substrates (5–25 Ω·cm) typically in use in advanced BiCMOS and CMOS process technologies, mainly result in poor performance of the passive elements. To lower the losses related to the substrate, the use of high ohmic silicon substrates with thick metallization schemes is considered one of the most promising routes to follow. Substituting low with high ohmic substrate material parameters yields very promising low-loss components [2]. Unfortunately, components realized in high ohmic silicon technology suffer from much higher losses than predicted by EM simulations. In addition, also a strong fluctuation in the losses over the wafer for identical components has been observed. This behavior can be correlated to the presence of a surface charge layer at the silicon-insulator interface. This surface charge layer gives rise to additional eddy currents and associated losses at microwave frequencies [3].

In this work we demonstrate that using a state-of-the-art Marchand-balun design, implemented in an optimized high-ohmic silicon technology for RF/ millimeter-wave applications, can overcome the problems related to the surface charge. This yields improved integrated passive components, which can compete with GaAs and alumina solutions even for K-band applications. Since advantages are most evident in the millimeter-wave region, we will present our results for coplanar waveguides and Marchand-type baluns at frequencies up to 30 GHz. With these two building blocks, we extract important information on propagation and losses in transmission lines and coupled lines, both widely used in circuits for telecommunication systems.

II. COPLANAR WAVEGUIDES

We have implemented 50 Finitc Ground Coplanar Waveguide (FGCPW) lines optimized for on wafer probing (Fig. 1). The transmission lines are intended for determination of the attenuation coefficient of HRS integrated transmission lines. FGCPW allows us to use compact dimensions without introducing significant disadvantages as compared to CPW design, this provided that some basic design rules are respected [4]. The measured results will be discussed in section V.

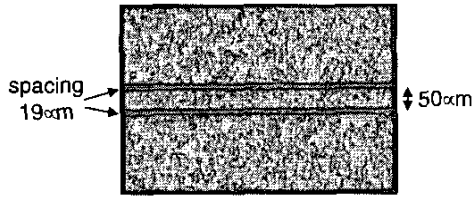

Fig. 1. One of the FGCPW lines used for the determination of the attenuation coefficient (500 x 488 $\propto m^2$). The metal layer is aluminum 3∝m thick.

III. MARCHAND BALUN

A. Theory

When designing a balun for perfect balance and wide-band performance, most coupled-lines based designs require a very high even-mode to odd-mode impedances ratio. This requirement is, however, not very compatible with integrated solutions. Marchand-type baluns [5]-[7] are more tolerant to lower even-mode impedance, facilitating the design of a broadband planar balun structure.

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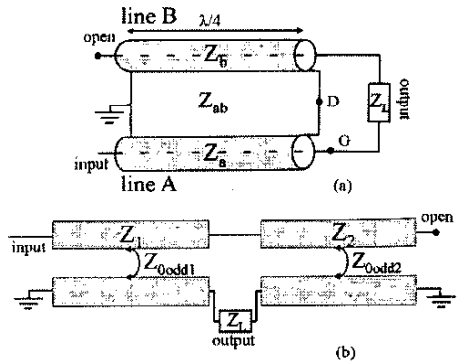

Fig. 2. Marchand balun in coaxial configuration (a) and using coupled lines (b).

The original Marchand balun is composed out of two λ/4 coaxial transmission lines (Fig. 2a). Since we aim for integration we follow the analysis of [6] to obtain a clear view on the design constrains of planar implementations. Using the equivalent circuit for the structure of Fig. 2a, it is possible to obtain an expression for the impedance between points D and G, yielding:

$$Z_{DG} = \frac{jZ_L Z_{ab} \tan\theta_{ab}}{Z_L + jZ_{ab} \tan\theta_{ab}} - jZ_b \cot\theta_b \qquad (1)$$

The impedance Z_{DG} is, in turn, transformed by line A to the input. At the resonance frequency we find (assuming $\theta_{ab} \quad \theta_b$) that $Z_{DG} = Z_L$ and $Z_{in} = Z_a^2 / Z_{DG}$. From (1) we can conclude that the bandwidth of the balun can be improved by making Z_{ab} large compared to Z_L. Under this condition, the relations above will be a good approximation in a wide frequency range, centered around $\theta =$ /2 [6,7].

B. Marchand baluns using coupled lines

In Fig. 2b a basic implementation of a planar coupled line Marchand balun is given with the related parameter mapping. In order to obtain a wideband Marchand balun, we fix Z_{0even} between 3 and 4 times Z_{0odd}. Furthermore, we will assume a simplified configuration where $Z_{0odd1} = Z_{0odd2}$. Consequently, we can achieve matching for a given value of input and output impedances using:

$$Z_{0odd} = \frac{1}{2}\sqrt{Z_{in} \cdot Z_L} \qquad (2)$$

Note that here, we make the implicit assumption that only the odd-mode will propagate due to the much higher impedance of the even mode.

From the above it is clear that the odd-mode and high even-mode impedance of the coupled lines, are the two basic design parameters for the Marchand balun. Equation (2) reveals also that, in a 50 system, the proper odd-mode impedance is rather small, resulting in a high capacitance between coupling lines, i.e. very narrowly spaced conductors. This condition must be avoided in practice, since it is sensitive to process variations and complicates the accuracy of the EM-simulations. Low odd-mode impedances can also be accomplished using a three-line solution, which relaxes the line spacing [7]. Since we aim for an on-wafer probeable structure, in order to obtain the highest accuracy during characterization, we implement the Marchand balun as a three coupled CPW line structure with a cross section as depicted in Fig 3.

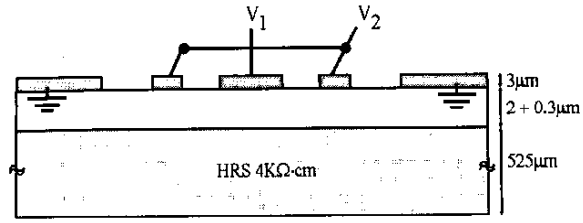

Fig. 3. Cross section of the three line configuration.

The design procedure used for the three coupled lines sections follows that of [7]. The objective here was to find the optimum geometrical configuration that satisfies the impedance constrains and, at the same time, provides a good balance between the width/spacing of the lines for minimum losses. A final optimization of the full layout was performed using an EM-simulator.

At the end sections of the coupled line structures we need connections between the finite ground planes to enforce a uniform ground along the circuit and to avoid the propagation of non-TEM modes. The required connections will also introduce some capacitive coupling between the signal lines and the ground planes (Fig 6). Initial EM simulations indicated a rather dramatic degradation of the balun matching and its wide-band behavior through this coupling. For this reason an extensive EM simulation study and technology optimization was performed in order to minimize these effects and to obtain a good balun performance.

IV. An Optimized RF/Millimeter-Wave Silicon Technology

A. Basic Process

We developed an in-house custom DIMES process to implement high quality passives with only 2 metal layers. The high ohmic substrate (4 k ·cm p-type) is 525 ∝m thick, with a dielectric constant of ε_r=11.7. The metal layers are aluminum respectively 2∝m and 3∝m thick, separated by 2∝m of oxide. Although a thicker oxide would be beneficial for the coupling to the ground bridges, it complicates the implementation of via connections

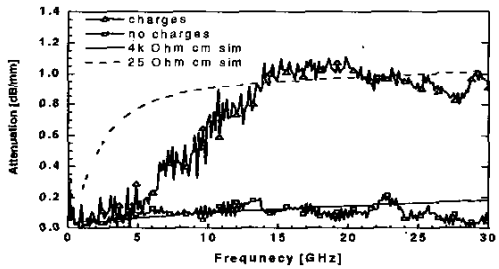

Fig. 4. Attenuation in dB/mm of the CPW lines using conventional process and with the surface charge suppression

between the metal layers, and negatively affect the wave propagation by its lower dielectric constant [8]. The first metal layer is separated from the substrate by a silicon oxide layer of 0.3 μm. If active devices are present, they must be placed in a locally implanted p-type well, to isolate them from the rest of the chip. In this case, particular attention must be devoted to obtain a sufficiently narrow depletion region of the junction. Without these changes, the integration on HRS is difficult or impossible.

B. Surface Charges

The influence of surface charge states on the loss properties of silicon integrated passives has been the subject of several pieces of work [9],[10]. However, the proposed solutions introduce major changes in the manufacturing process. Our method to reduce the effects of the charged states at the silicon-insulator interface is based on the selective implant of argon in the substrate regions under the integrated passives. This implant is designed to completely amorphize the silicon surface. The efficiency of this process has also been demonstrated in a process for integrated passives [11]. In our case the compatibility with active device processing demands that all high temperature treatments are completed before the argon implantation to avoid recrystallization of the amorphous region. Therefore a high energy implant and special masking of the active device regions was developed. C-V measurements showed that any mobile charge at the interface of the high-resistivity wafer, either from the inherent surface charge under the oxide or from doping contamination during active device processing, has been almost completely deactivated by this process step. In this way our technique is fully compatible with the conventional BiCMOS process technology and the advantages at microwave frequencies are significant, as will be shown in the following section.

V. Experimental Verification

A. The Co-planar Lines

To demonstrate the effects of the additional processing

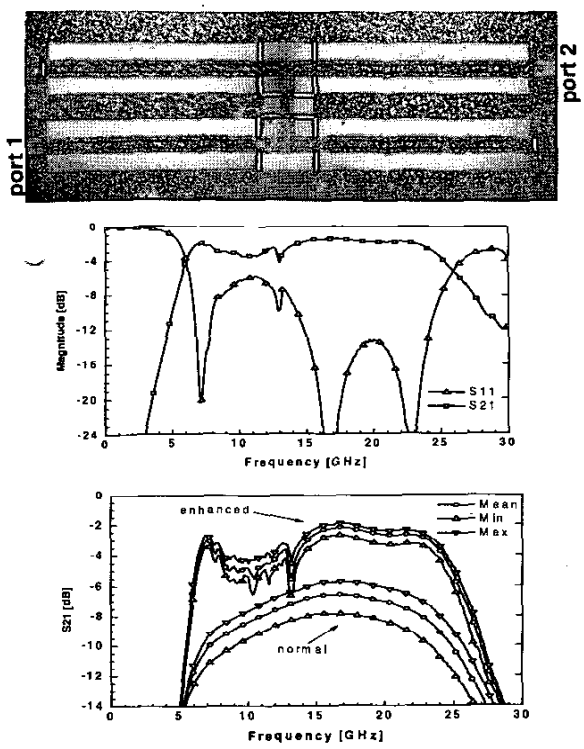

Fig. 5. Picture of the fabricated back-to-back balun configuration (4.4 x 1.6 mm^2) and 2-ports S-parameters results over the wafer, with and without the surface charge suppression.

steps for surface charge suppression, we consider the measured attenuation constant of a 50 Ω CPW line fabricated using conventional HRS technology (Fig 4). The same line geometry was also implemented with the add-on process module. In the first case the presence of charge at the silicon–silicon dioxide interface is responsible for the additional losses at higher frequencies. Above 10 GHz, the attenuation constant behaves as if the line is implemented on a substrate with a much lower resistivity (~25 Ω·cm). Using the additional surface charge suppression, a dramatic improvement in loss reduction is observed. The attenuation for the same line geometry has been reduced to below 0.2dB/mm up to 30GHz.

B. Balun 2-Ports Measurements

One of the most practical and reliable methods to accurately investigate the metal and substrate losses in balun structures is the use of a back-to-back configuration of 2 baluns, as illustrated in Fig. 6. Since the second balun is matched to the first one, possible imbalances will be canceled. The obtained results set the upper limit of the balun performance. The back-to-back Marchand balun structure, based on 25 μm coupled lines implemented with

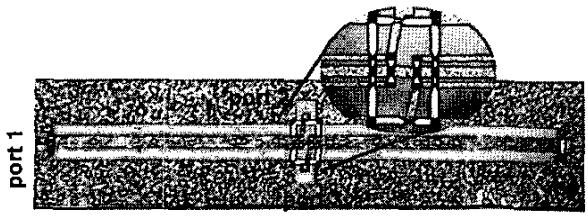

Fig. 6. Picture of the fabricated 3-ports configuration (4.3 x 1.3 mm^2) and detailed view of the coupled line end-sections.

the modified HRS technology, has a remarkable performance. Fig. 6 shows that the measured insertion loss is about 1.5 dB at the center frequency of 17.7 GHz for the total structure, therefore the loss related to a single balun is less than 0.8 dB, this without even taking into account the losses of the connections between the two structures. The return loss is typically better than 10 dB between 15 GHz and 25 GHz. We present also the statistics over the wafer for the same balun configuration. A clear improvement of more than 2 dB is observed. Since the presence of surface charge is fluctuating over the wafer, large variations are found for the insertion loss if no measure against this surface charge is applied. Using the additional processing module the fluctuations are significantly reduced. From Fig 6 it can be noted that an effective high ohmic substrate involves a more unstable s_{21}. This can be explained by the fact that the substrate presents not only lower losses for the fundamental TEM mode, but also for additional parasitic modes, which are free to propagate.

C. Balun 3-Ports Measurements

The balun matching and balancing was confirmed through a 3 ports measurement using a two-port network analyzer. The correction procedure was introduced by Tippet at al. [12] and later simplified in the analytical formulation by Dropkin [13], in order to reduce the inaccuracy related to the mathematical manipulations of the measured data. The results are summarized in Fig. 7. It must be noted that the insertion loss of a balun in a 3-port measurement will be slightly higher than for the back-to-back balun configuration. This can be explained by impedance miss-match of the balanced ports, 60 rather then the desired 50 . This level can be confirmed through S-parameter analysis of the measured data. In addition, this configuration is loaded with the parasitics related to the single-ended wafer probe outputs. The phase unbalance has a minimum at lower frequency, a behavior that has been reported also by other authors [14].

V. CONCLUSIONS

In this work we have applied a novel processing module to reduce the effects of surface charge on integrated passives in high ohmic silicon. With this innovation high

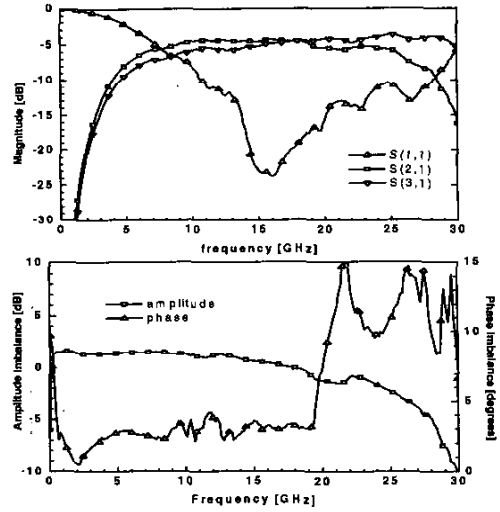

Fig. 7. Measured 3-ports S-parameters, amplitude and phase imbalance of the Marchand balun in the 3-ports configuration.

resistivity silicon has unquestionable advantages for low-cost fully integrated on-chip RF/microwave solutions. The losses found for integrated passives are comparable with state-of-the-art GaAs implementations, while maintaining compatibility with the conventional silicon technology. Excellent results were obtained for the coplanar waveguides and Marchand baluns for Ka-band applications. In particular, the Marchand balun (50 unbalanced, to 50 balanced) has, to the knowledge of the authors, the lowest insertion-loss ever published for high ohmic silicon at these frequencies.

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